REMARKS

I. Introduction

Applicants and Applicants representative would like to thank Examiner Ghulamali again for the indication of allowable subject matter recited by claims 2-4.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claim 1 Under 35 U.S.C. § 103

Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over USP No. 5,757,857 to Buchwald in view of USP No. 5,123,030 to Kazawa, and further in view of USP No. 4,453,084 to Brouwer. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites in-part a clock recovery circuit comprising a phase error detection part including a selection part for selecting, according to the detected variation pattern, whether the estimated phase error is output to the control part.

In the pending rejection, the Examiner admits that Buchwald and Kazawa do not disclose the aforementioned claimed limitation, and the direction selection circuit 125 of Brouwer is relied upon to cure this defect of Buchwald and Kazawa.

However, Applicants respectfully disagree with such interpretation, because Brouwer expressly discloses that the direction selection circuit 125 develops a blocking signal that selectively blocks either the first or the second pulse appearing in the switching logic 115 from the line center detector 107 through line 116, where the selection of the first or the second pulse is ***dependent*** upon which of the directional switches 119/120 on the control panel 106 is pre-selected by the operator (see, col. 9, lines 23-32). Accordingly, it is respectfully submitted that the direction selection circuit

125 of Brouwer does not select according to the alleged detected variation pattern or the pattern detection circuit 183. This is further evidenced by the fact that the direction selection circuit 125 does ***not*** receive any signal from the pattern detection circuit 183, let alone determine whether the alleged estimated phase error is output based on such signal. Most importantly, the pattern detection circuit 183 detects a geometric pattern 13 to be traced (see, Fig. 1). That is, even assuming *arguendo* that the direction selection circuit 125 receives an electrical signal from the pattern detection circuit 183, such signal does not allow the direction selection circuit 125 to determine whether the alleged estimated phase error is output to the alleged control part.

For all of the foregoing reasons, it is respectfully submitted that Brouwer does not disclose or suggest a selection part for selecting, according to the detected variation pattern, whether the estimated phase error is output to the control part, as recited by claim 1.

Furthermore, Applicants note that the Examiner has not expressly identified the ***inter-relationship*** between the direction selection circuit 125 of Brouwer, the alleged control part (i.e., low pass filter 58) of Buchwald and the estimated phase error output from the alleged phase error estimation part (i.e., phase comparator 80) of Kazawa. Accordingly, even further assuming *arguendo* that the proposed combination discloses the claimed invention, it is respectfully submitted that the proposed combination is improper because the pending Office Action has not provided the requisite ***objective*** evidence ***from the prior art*** that "suggests the desirability" of the proposed combinations. As such, it is respectfully submitted that the rejection relies solely on improper hindsight reasoning, whereby the rejection has selected bits and pieces of the prior art and used only Applicants' specification inadvertently as a guide to reconstruct the claimed invention. For example, it is alleged that "it would have been obvious ... to use a selection circuit ... as taught by Brouwer in the circuit of Buchwald and Kazawa so as to achieve proper clock recovery." However,

the objection of the high speed self-adjusting clock recovery circuit of Buchwald is to recover the clock signal based on the NRZ data bit stream (e.g., by detecting the edge transitions of the NRZ data bit stream, see, col. 5, lines 17-19), so that the alleged motivation (i.e., clock recovery) is already achieved by prior art.

At best, the pending Office Action has attempted to show only that the elements of the claimed invention are ***individually*** known without providing a *prima facie* showing of obviousness that the ***combination*** of elements recited in the claims is known or suggested in the art. That is, the Examiner identifies that the direction selection circuit 125 of Brouwer selects according to the pattern of the pattern detection circuit 183 without addressing ***how*** such a selection is related to the alleged control part (i.e., low pass filter 58) of Buchwald and the estimated phase error output from the alleged phase error estimation part (i.e., phase comparator 80) of Kazawa.

Thus, for these additional reasons, Applicants respectfully submit that the combination of cited prior art references is improper and should therefore be withdrawn.

III. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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